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ANALOG TO DIGITAL CONVERTER IN DIGITAL PROTECTIVE RELAYS

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CONVERTOR ANALOG-DIGITAL ÎN RELEE DIGITALE DE PROTECȚIE

The accuracy and the speed of decision making of the protection relays are very important to maintain the continuity of supply to the electrical power system during different disturbances.

A/D Converter shares an important role in achieving that requirement, so that all types of A/D Converters used in power relaying applications will be discussed in this paper and some recommendations will be offered depending on that discussion.

Acuratețea și viteza de luare a deciziilor a releelor de protecție sunt foarte importante pentru a menține continuitatea aprovizionării sistemului de energie electrică în timpul diferitelor perturbații.

A/D convertorul analog-digital are un rol important în realizarea acestei cerințe, astfel încât toate tipurile de convertoare A/D utilizate în transmiterea aplicațiilor de putere vor fi discutate în această lucrare și unele recomandări vor fi oferite în funcție de această discuție.

Keywords: digital relay, digital signal processing, electrical power system, digitization, quantization, sampling

Cuvinte cheie: releu digital, procesare a semnalului digital, sisteme de energie electrică, digitizare, cuantizare, eșantionare

1. Introduction

Analog to digital converter is used to convert the analog input signals, voltage and currents obtained from VT and CTs, from analog form to digital form.

Digitization involves two processes: sampling (digitization in time) and quantization (digitization in amplitude).

The resulting samples are fed to the digital signal processor (DSP) where the Relay algorithms (digital filter) process these signals and they issuing orders to the circuit breakers to isolate the specific defect element selectively for maintaining the continuity of feeding in the rest of the system and the safety of equipment and personnel [1], [2], [3].

2. Digital Relay Structure

As shown in Figure 1, Numerical relay consists of the following main components:

- Independent power supply.
- Analog inputs: provides galvanic isolation for the relay from the power system [10].
- A surge filter: is used to limit the excess inrush in the input signals, for the safety requirements of a numerical relay [1], [2], [3].
- Low pass filter (An anti-aliasing filter) (LPF): is designed to suit a specific choice of sampling rate used [4].
- Multiplexer: is a set of analog switches, connect each of the input signals in turn, according to the Analog Input Subsystem, either to the A/D converter or to the sample-and-hold circuit.
- Sample and Hold Circuits: are used to sample an analog signal and to hold (store) its value for some length of time until the A/D converter can process the information.
- Sampling Clock: used to synchronize all sampling of voltages and currents throughout the system, and having a common reference for all the phasors computed in the substation [4], [7], [8], [9], [10].
- Analog / Digital filter (A /D).
- Microprocessor.
- Random Access Memory (RAM): is used to capture the input sample data as they are processed. Also, RAM is used as a

memory book or for storing data temporarily, during relay algorithm implementation [1], [4],[10].

- Programmable Read Only Memory (ROM/PROM): is used to save the programs permanently [1], [4], [10].
- The Erasable PROM (EPROM): is required for saving and storing the relay settings, which may be changed once a while [1], [4], [10].
- Digital Output System: is provided with optical isolators which secure complete physical isolation between the relay and the power system [1], [4], [10]. Figure 1 shows the block diagram of a Numerical relay.



Fig. 1 Typical functional block diagram of a numerical relay

3. Digitization and Quantization

Any binary number for example 11100111(231 in decimal), we can send it as a string of data of a network in two ways, either from left to right as Most Significant Bit First (MSB) or from right to left as Least Significant Bit First (LSB)[4].

Digitization is defined as A process that mapping a continuous range of values of an input signal into limited set of possible values, so that the output signal is discrete in time and amplitude[12], [14].

The number of possible values that the converter can output is 2^{N} , where N is the number of bits in the AD converter i.e., for a 3-bit A/D converter. The number of possible values is 2^{3} =8.

Analog quantization size: If we have 0-10V signals.

Separate them into a set of discrete states with 1.25V increments as shown in table 1 and which is calculated according to the following equation:

$$Q=(Vmax-Vmin) / 2^{N} = (10V - 0V)/8 = 1.25V$$
 (1)

Output States	Discrete Voltage Ranges (V)
0	0.00-1.25
1	1.25-2.50
2	2.50-3.75
3	3.75-5.00
4	5.00-6.25
5	6.25-7.50
6	7.50-8.75
7	8.75-10.0

Table 1

The maximum step error acceptable in analog-to-digital converter is e $_{max}$ =1/2 LSB in magnitude.

Let us suppose that the output value must equal 110.49, but the output is 110 or 111 both of them are correct, that mean we have 0.5 LSB error and these values are within the acceptable limits [4], [14].

As a rule, for *N*- bits ADC, and the maximum input voltage for the ADC is *V* volts, the quantization error is defined by the equation [2]:

$$q = \frac{V}{2^{N}} \tag{2}$$



Fig. 2 Quantization errors of ADC

From the previous equation and equation (2), whenever the number of bits of the ADC is larger, the quantization error is less.

The main characteristics of the A/D converter are determined by the following parameters [5], [4], [12]:

- The word – length(m), it's the number of bits (m = 8...12...16 bits) of the A/D converter, a bit is the smallest possible meaningful piece of information and in the binary numeral system: either 0 or 1, A string of 8 bits is called a byte.

- The range of converter M or the range of the analog input signal.

- Conversion Speed: The number of samples (bits) converted from Analog to Digital form in a second [11].

Many types of ADCs depend on the method of the conversion process, such as: Flash ADC, Successive approximation ADC and Delta-sigma ADC.

4. Flash ADC

Figure 3 shows flash ADCs with *N*-bit resolution that has $2^{N} - 1$ comparators, the basic architecture of a flash ADC consists of three components [11], [12], [13]:

- A voltage divider network: is a network of identical resistors which are connected together according to the voltage divider rule; if every resistor has an identical value of other resistors it will have also an identical voltage drop across it. Well, we've got here is the reference voltage (Vref). From figure 3, the reference voltage is 8V and the voltage drop at every resistor is 1V, after the first resistors it should get 7V, 6V, 5V, 4V, 3V, 2V and 1V.
- A bunch of comparators: each comparator compare between the values of reference voltages (Vref) with the analog input voltage(Vin), if Vin is greater than Vref the output of that comparator is a high or true or equal 1 and if Vin smaller than Vref the output of that comparator is a low or false or equal 0.
- A priority encoder-logic unit: generates a binary number based on the highest-order active input, ignoring all other active inputs. From figure 3, there are many inputs for the encoder(5V, 4V, 3V, 2V, 1V), but because it's apriority input (5V) ignoring those lower inputs, so five is the highest-order active input and the output Binary Equivalent is 101.



comparators are required and for 8- bit 255 comparators are required.

- Expensive.
- Lower resolution.

5. Successive approximation ADC

This thing can be done by converting an analog signal into digital signal by using binary search through all possible quantization levels before finally converting upon a digital output for each conversion. From figure 4, a successive approximation A/D converter consists of four main sub-circuits [6], [12], [14]:

1 - comparator: compares the applied input voltage (V in) against the output of an N-bit DAC (V out). The result of the comparison is a serial data input to the successive approximation register (SAR).

2 – successive approximation register (SAR): is esigned to supply an approximation digital code of V into the internal ADC. This register counts by trying all values of bits, starting with the MSB and finishing at the LSB.

3 - A DAC converter in a feedback loop.

4 - output latches circuit: The latch circuit at the end of conversion holds onto the resultant digital data output.



Fig. 4 Successive approximation A/D converter [6], [12], [14]

The conversion algorithm is as follows, Initially all *n* bits are reset to zero in the SAR, so that the most significant bit (MSB) b_B is set to equal a digital 1, each bit is set to 1 in sequence[6]. The newly formed binary number is fed to the DAC, which then supplies the analog equivalent voltage of this binary number to the comparator subcircuit for comparison purpose with the sampled input voltage.

If the DAC output (V out) exceeds the sampled input voltage (V in), then the comparator causes the SAR to that bit to zero(off); Otherwise, the bit will be left a 1(*on*).

This process is repeated until every bit in the SAR has been tested. The SAR will hold the correct bit vector b = [b1, b2, ..., bB],

which is then latched(sent) on to the output. The resultant code is the digital approximation of the sampled input voltage [6], [12], [14].

Advantages [12], [13], [15], [16]:

- Capable of high speed and reliable.
- Medium accuracy.
- Good tradeoff between speed and power.

Disadvantages [12], [13], [15], [16]:

- Complex design.
- Expensive.

6. Delta-sigma ADC

From A block diagram of a sigma-delta converter illustrated in Figure 5, a delta-sigma ADC consists of Integrator, a 1 bit analog to digital converter, digital low-pass filter, digital decimation filter and a 1 bit digital to analog converter in a feed-back loop.

Over- sampled input signal x1 goes to the integrator to be integrated in it and the output of the integrator x2 is fed to the 1 bit ADC.

The purpose of using feed-back circuit is to certify that the analog input signal and the converted signal are identical.

After a series of iterations, summing junction produces a serial bit stream proportional to input voltage V_{in}.

A digital low-pass filter converts the 1 bit data stream to a multibit data stream, to remove frequency components at or above the Nyquist frequency, a decimation filter is used to get the sampling rate of interest in relaying applications[4], [12], [14].



Fig. 5 Sigma-delta ADC [4], [12]

Advantage [4], [12], [14]: low cost, low power and high-resolution conversion.

Disadvantage [4], [12], [14]: low speed conversion due to oversampling and ADC circuit is somewhat complex.

7. Conclusion

■ Each components of digital relay unit needs a lot of study and analysis, because the total performance of the digital relay is integrated.

■ Analytical and simulation tools which have real models must be used to get results too close to the practice as much as possible.

■ Through comparisons between different types of A/D Converters, the new generation must be low power consumption, high speed and high accuracy, to achieve the better performance of digital relays.

REFERENCES

[1] * * * Network Protection & Automation Guide, Edition MAY 2011, Published by Alstom Grid ISBN: 978-0-9568678-0-3.T

[2] T.Davies, Protection of Industrial Power System, Published by Elsevier Ltd, USA, 2006.GGMNNBX

[3] * * * On Power Quality And Protection, Technical Report No. 372L, Chalmers University of Technology, Sweden, March, 2001.

[4] Arun G. Phadke, James S. Thorp, Computer Relaying For Power Systems, second edition, USA, 2009.

[5] T.S. Sidhu, M.S. Sachdev, M. Hfuda, computer simulation of protective relay designs for evaluating their performance, IEEE, University of Saskatchewan, CANADA, 1996.

[6] Edmund Lai, Practical Digital Signal Processing for Engineers and Technicians, IDC Technologies, Great Britain, 2003.

[7] Wei-Ming Wu, Fan-Tien Cheng and Fan-Wei Kong, Dynamic-Moving-Window Scheme for Virtual-Metrology Model Refreshing, IEEE RANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 25, NO. 2, MAY 2012.

[8] Insoo Kim, Kyusun Choi, Sample & Hold Circuits, The Pennsylvania State University, 2011,USA.

[9] Zjajo, Amir, Pineda de Gyvez, Jose, Low-Power High-Resolution Analog to Digital Converters, Springer, 2011.

[10] *** Terms Used by Power System Protection Engineers, Prepared By The IEEE Power System Relaying Committee, Relay Standards Subcommittee and Power System Engineers Working Group, The Institute Of Electrical And Electronic Engineers, IEEE,2013.

[11] M. Subba Reddy, S. Tipu Rahaman, An Effective 6-bit Flash ADC using Low Power CMOS Technology, IEEE, 2013.

[12] * * * IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Instrumentation & Measurement Society, IEEE Std 1241, USA, 2011.

[13] S., Daponte, P., Balestrieri, E., De Vito, L., Tilden, S. J., Max, S., and Blair, J., "ADC Parameters and Characteristics," IEEE Instrumentation and Measurement Magazine, vol. 8, no. 5, pp. 44–54, Dec. 2005 [B46], 2005 IEEE.

[14] Sophocles J. Orfanidis, introduction to Signal Processing, Rutgers University, USA, 2010.

[15] Olli Kursu and Timo Rahkonen, Charge Scaling IO-bit Successive Approximation AID Converter with Reduced Input Capacitance, IEEE, FINLAND, 2011.

[16] Gustavo Della Colletta, Luis H. C. Ferreira and Tales C. Pimenta, A Low Power Successive Approximation A/D Converter based on PWM technique, Brazil, 2014.

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